DOLPHIN

DESIGN

New Features

SMASH 7.5.2 - SCROOGE 4.5.2 - SHAKER 7.5.2

May 4, 2020

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Preamble

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to support@dolphin.fr with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be assured that we will try to take it into account in a future release.

Web Site

Our web site www.dolphin-design.fr is a source of information on our EDA solutions. Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

Supported Platforms

Microsoft Windows

SMASH is designed to run on Microsoft Windows Vista / 7 / 8 / 10 on x86_64 platforms.

Linux on Intel x64 platform

SMASH is designed to run under X-Window on RedHat Enterprise Linux 6 (RHEL6) and supports compatible Linux distributions on x86_64 platforms.

Credits & Copyrights

wxWidgets: A free C++ framework for cross-platform programming

http://www.wxwidgets.org

wxWindows Library License, Version 3

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This product includes cryptographic software written by Eric Young. This product includes software written by Tim Hudson.

Original SSLeay License

Copyright 1995-1998 Eric Young

All rights reserved.

This package is an SSL implementation written by Eric Young. The implementation was written so as to conform with Netscapes SSL.

This library is free for commercial and non-commercial use as long as the following conditions are aheared to. The following conditions apply to all code found in this distribution, be it the RC4, RSA, lhash, DES, etc., code; not just the SSL code. The SSL documentation included with this distribution is covered by the same copyright terms except that the holder is Tim Hudson.

Trio: portable and extendable printf and string functions

Gear-Brayton Integration Method

The new formulation of the Gear-Brayton integration method included in SMASH was perfected and implemented at Supélec - Service des Mesures.

EKV3 Compact MOSFET Model Documentation

A. Bazigos, M. Bucher, F. Krummenacher, J.-M. Sallese, A.-S. Roy, C. Enz, "*EKV3 Compact MOSFET Model Documentation, Model Version 301.01*", Technical Report, Technical University of Crete, November 23, 2007.

VDA / FAT Open Source Library

The open source library of VHDL-AMS components created by the VDA / FAT working group is delivered with SMASH.

The VDA / FAT Working Group AK 30 "Simulation of Mixed Systems with VHDL-AMS" is organized within the Association for Research in Automobile Technology (FAT - Forschungsvereinigung Automobiltechnik) of the German Association of the Automotive Industry (VDA - Verband der Automobilindustrie). It promotes the relationship between car manufactures and their suppliers concerning simulation of mixed systems and model exchange.

The working group promotes the development of VHDL-AMS models that are integrated in different libraries.

FUNDAMENTALS_VDA

Public library with general VHDL-AMS models like time sources, converters between different domains, table-lookup models, relays, switches...

SPICE2VHD

VHDL-AMS models with nearly the same terminal behavior like Spice models of basic electrical elements like resistor, capacitor, inductor, and level1 models of semiconductor devices.

AUTOMOTIVE_VDA

Library under development with special parameterized models like wires, fuses, bulbs, EMC test signals...

New Features

SMASH - Documentation

Enhancements

- Documented aging html results file generated for TMI aging simulations (DDIsa13598 - SMASH 7.5.0)

SMASH - Kernel

Enhancements

- Improved transient statistic information details displayed in output log file (DDIsa13587 - SMASH 7.5.0)
- Modified report loading file for models defined in subckt (DDIsa13594 - SMASH 7.5.0)
- Improved the multi-thread performance by applying it on more SPICE devices (DDIsa13630 - SMASH 7.5.0)
- Improved LTE (Local Truncation Error) algorithm to get best ration speed-up/accuracy during transient analysis (DDIsa13676 - SMASH 7.5.1)
- Improved the writing time of binary operating-point file for big flatten netlists (DDIsa13888 - SMASH 7.5.1)
- Provided an option to apply the net multiplicity on the capacitance added by the .CAPAMIN directive (DDIsa13919 - SMASH 7.5.1)
- Implemented a new option to short DC voltage sources (DDIsa13944 - SMASH 7.5.1)
- Modified the default value of RM_RMIN option to enable it (DDIsa13971 - SMASH 7.5.2)

Bug fixing

- Corrected the CPU consumption when the multi-thread is activated (DDIsa13596 - SMASH 7.5.0)
- Corrected the evaluation of resistors that are below 'RESMIN' value and shorted by .CONNECT directive (DDIsa13643 - SMASH 7.5.0)
- Corrected output thermal noise computing with SPARSE solver of bipolar and several MOSFET models (DDIsa13913 - SMASH 7.5.1)
- Corrected a crash that could occur with Z instances and the SPARSE solver (DDIsa13935 - SMASH 7.5.1)
- Corrected singular matrix management with NICSLU solver (DDIsa13966 - SMASH 7.5.2)
- Corrected a crash occurring when a X instance with an unconnected port was merged (DDIsa14000 - SMASH 7.5.2)

SMASH - Models

Enhancements

- Improved the performance of SPICE devices with dynamic formula (DDIsa13739 - SMASH 7.5.0)
- Implemented additional AC transfer functions on voltage controlled sources (DDIsa13779 - SMASH 7.5.0)
- Implemented support of transient noise analysis for TMI (TSMC Model Interface) models (DDIsa13313 - SMASH 7.5.1)
- Updated BSIM-BULK 106.2 with august 2019 TSMC changes (DDIsa13549 - SMASH 7.5.1)
- Improved MOS regions information displayed in OP file by adding details about weak/strong inversion and "no saturation"/saturation/linear region (DDIsa13833 - SMASH 7.5.1)
- Improved simulation speed-up of BSIM4 models with drain/source access resistors (DDIsa13862 - SMASH 7.5.1)
- Improved the convergence of SPICE BJT model (DDIsa13891 - SMASH 7.5.1)
- Improved generated compact model to avoid noise convergence problem due to sqrt function (DDIsa13899 - SMASH 7.5.1)
- Improved swift method using by MOS transistors model to speed-up simulations (DDIsa13974 - SMASH 7.5.2)

Bug fixing

- Corrected computations of ID, VDS, VBS, VGS output variables for MOS transistors in advanced technology nodes (DDIsa13832, DDIsa13524 - SMASH 7.5.1)
- Corrected the computation of some variables of BSIM4 and BSIM3 SPICE models when MOS are merged (DDIsa13847 - SMASH 7.5.1)
- Corrected the merge mos option for PSP102, PSP103, EKV3, UTSOI-V114, UTSOI-V210 and UTSOI-V220 models (DDIsa13848 - SMASH 7.5.1)
- Corrected evaluation of CCVS and CCCS sources that depends on the current of H or E sources (DDIsa13857 - SMASH 7.5.1)
- Corrrected transient noise simulation divergence caused by R3CMC SPICE model (DDIsa13892 - SMASH 7.5.1)
- Corrected the instance output noise and nze report file of SPICE models (MOS and BJT) that have access resistors (DDIsa13893 - SMASH 7.5.1)
- Corrected access resistance value for inductance when multiplicity differs from the value 1.0 (DDIsa13911 - SMASH 7.5.1)
- Corrected a crash that could occur with Y instances and '.CONNECT' or 'RM_RMIN' options (DDIsa13940 - SMASH 7.5.1)

SMASH - SPICE

Enhancements

- Improved ALLGMIN OP stepping algorithm and implemented GSHDC stepping (DDIsa10308 - SMASH 7.5.0)
- Implemented a formula function for 2D interpolation from waveforms (DDIsa13780 - SMASH 7.5.0)
- Implemented support of new analog solver multi-threadings NICSLU to speed-up analog simulations (DDIsa13571 - SMASH 7.5.1)
- Improved the simulation runtime by providing an option to merge identical X instances in parallel (DDIsa13842, DDIsa13722 - SMASH 7.5.1)
- Improved simulation speed-up of large SPICE circuits by merging identical bipolar transistor in parallel (DDIsa13903 - SMASH 7.5.1)
- Implemented S and Y access functions for 2 ports circuits (DDIsa13932 - SMASH 7.5.1)
- Implemented new CGND option to improve simulation speed of post-extraction netlists decoupling small capacitors (DDIsa13948 - SMASH 7.5.1)
- Implemented .BIASCHK directive support for "SUBCKT" syntax (DDIsa12122 - SMASH 7.5.2)

Bug fixing

- Corrected the sort of pwl / table values within SPICE formulas (DDIsa13723 - SMASH 7.5.0)
- Corrected the display of error messages when table2d function use an incorrect wave file (DDIsa13867 - SMASH 7.5.1)
- Corrected a wrong warning message while user launches transient noise analysis and power-up enabled (DDIsa13898 - SMASH 7.5.1)
- Corrected potential unwanted HZ output message in log file during OP analysis (DDIsa13958 - SMASH 7.5.1)
- Corrected OP measurements which are not to be executed while operating point fails to converge (DDIsa13981 - SMASH 7.5.2)

SMASH - Verilog-AMS

Enhancements

- Modified the Verilog-AMS parser to allow the 'limexp()' analog operator within a conditional statement with non constant condition (DDIsa13537 - SMASH 7.5.1)

Bug fixing

- Corrected an elaboration error when a Verilog-AMS voltage source is shorted to the ground (DDIsa13649 - SMASH 7.5.0)

SMASH - Viewer

Enhancements

- Improved use of the evaluation option license by opening the Dolphin Solutions download page at startup (DDIsa13809 - SMASH 7.5.0)

Bug fixing

- Corrected the behavior of keyboard usage when editing a bookmark name (DDIsa13515 - SMASH 7.5.0)
- Corrected a crash on VCD file dispayed with logic real signal (DDIsa13785 - SMASH 7.5.0)